ATS 2022

Date	Time			
NOV 21	12:00	Registration Desk Open		
	13:30	**Tutorial 1 Part 1** Si-Based Qubits and Cryo-CMOS Control Circuits Jiun-Yun Li (Laurel Ballroom Salon I)	**Tutorial 2** Addressing Test, Safety, & Security for Connected Automotive ICs Lee Harrison and Wu Yang (Laurel Ballroom Salon II)	
	14:50	Break		
	15:10	**Tutorial 1 Part 2** Test and Diagnosis of Quantum Circuits James C. M. Li (Laurel Ballroom Salon I)	**Tutorial 2** Addressing Test, Safety, & Security for Connected Automotive ICs Lee Harrison and Wu Yang (Laurel Ballroom Salon II)	
	16:30	Break		
	17:30	Welcome Reception (Caf'e Laurel)		
NOV 22	08:00	Registration Desk Open		
	08:40	Plenary session		
	09:00	**Keynote 1** How the Test Community can Rise to the Challenge of Chiplets Jeff Rearick / Senior Fellow, AMD (Laurel Ballroom)		
	09:50	Break		
	10:00	**Keynote 2** Learning by Failing: Test-Thinking for Impactful Machine Learning Trista Chen / Director, Microsoft (Laurel Ballroom)		
	10:50	Break		
	11:10	**Keynote 3** A Paradigm Shift; From Device to System Testing Daniel F. J. Yang / Director, TSMC (Laurel Ballroom)		
	12:00	Lunch Break (Peony Ballroom)		
	13:30	**Industry Session 1** Latest Technologies and Solutions for Hyperscaler Designs (Laurel Ballroom Salon I)	**Regular Session 1** Reliable Designs (Laurel Ballroom Salon II)	**Regular Session 2** Secure Scan Chain (Chung Kang Room and Wen Hsin Room)
	14:30	Break		
	14:40	**Industry Session 2** Driving Intelligent System Design with 3D-IC (Laurel Ballroom Salon I)	**Regular Session 3** Measurement and Calibration for Test (Laurel Ballroom Salon II)	**Regular Session 4** Aging and Reliability (Chung Kang Room and Wen Hsin Room)
	15:40	Break		

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NOV 22	16:00	**Industry Session 3** The Test Solutions Addressing the Scalings for Technology, Design and System (Laurel Ballroom Salon I)	**Regular Session 5** Diagnostic and On-line Tests (Laurel Ballroom Salon II)	**Regular Session 6** System Security and Trust (Chung Kang Room and Wen Hsin Room)
	17:00	Break		
	18:00	Banquet (Laurel Ballroom)		
NOV 23	08:00	Registration Desk Open		
	08:30	**Industry Session 4** From Chip D&T to Energy-Efficiency (Laurel Ballroom Salon I)	**Regular Session 7** Advanced Test Generation Methods (Laurel Ballroom Salon II)	**Regular Session 8** Machine Learning and Test AI (Chung Kang Room and Wen Hsin Room)
	09:30	Break		
	09:40	**Special Session** Radiation Effects, Test, and Fault Tolerance (Laurel Ballroom Salon I)	**High School Posters** (Laurel Ballroom Salon II)	**Regular Session 9** Error Analysis and Tolerance (Chung Kang Room and Wen Hsin Room)
	10:40	Break		
	11:00	**Ph.D. Thesis Competition** (Laurel Ballroom Salon I)	**High School Posters** (Laurel Ballroom Salon II)	
	12:00	Lunch Break (Laurel Ballroom)		
	13:00	Social event		

Tutorial 1 - Part 1

Time: 11/21 13:30-14:50pm
Topic: Si-Based Qubits and Cryo-CMOS Control Circuits
Speaker: Jiun-Yun Li / Professor, National Taiwan University
Location: Laurel Ballroom Salon I

Abstract:
Si-based spin qubits are a promising platform for high-fidelity quantum computers for their scalability and VLSI compatibility due to the long spin decoherence. To achieve large-scale quantum computers, cryo-CMOS circuits is required to avoid issues by the electronic controllers at room temperature. Si-based qubits > 1 K enables a quantum system-on-chip (QSOC) including qubit processors and cryo-CMOS controllers. In this tutorial, fundamentals of Si-based qubits will be introduced first, such as material growth, device physics, and spin control/readout. Then the current progress and perspectives of Si-based qubits will be given, followed by the introduction of cryo-CMOS devices and circuits to access to qubits.

Outline:
- Introduction of Si-based qubits
- Materials and physics of Si quantum dots
- Characterization of Cryo-CMOS and circuits

Tutorial 1 - Part 2

Time: 11/21 15:10-16:30pm
Topic: Test and Diagnosis of Quantum Circuits
Speaker: James C. M. Li / Professor, National Taiwan University
Location: Laurel Ballroom Salon I

Abstract:
Quantum circuits (QC) are becoming an important computational technology in many useful applications, such as machine learning, optimization, and cryptography. Testing QC, however, is completely different from testing classical circuits. In this tutorial, we will introduce basic concepts about QC from test engineers' perspective. Then, we will introduce error, noise, and fault models for quantum circuits. Finally, we will propose new test generation and diagnose techniques for quantum circuits.

Outline:
- Basic Concepts about Quantum Circuits
- Errors, Noise, and Faults
- Test and Diagnosis of Quantum Circuits

Tutorial 2

Time: 11/21 13:30-16:30pm
Topic: Addressing Test, Safety, & Security
for Connected Automotive ICs
Speakers: Lee Harrison / Siemens EDA
Wu Yang / Siemens EDA
Location: Laurel Ballroom Salon II

Abstract:
The exponential growth of electronics in automobiles have stimulated significant innovation towards the development of advanced safety mechanisms. At the same time, automotive ICs are being manufactured in smaller technology nodes, which means maintaining high quality and reliability continues to challenge the safety targets.
As we rise to these new challenges for test, safety and security it has inevitably resulted in advances in the technology we deploy to detect and monitor defects as well as anomalies in both the silicon and the system. Coupled with the requirement to continue this monitoring for the life cycle time of the device rather than at just the manufacturing stage.
This tutorial aims to address the challenges of developing an automotive IC and walk through in detail how advanced test technologies can be used to address these challenges, before looking at the requirements of In-life monitoring and the impact this has on security . Highlighting some of the technologies that can be used to extract data from these automotive devices, safely and securely.

Outline

Part 1 - Introduction
Part 2 - High quality manufacturing test
Part 3 - Functional safety
Part 4 - SLM and In-Life Monitoring
Part 5 - Summary

Keynote 1

Time: 11/22 9:00-9:50am
Topic: How the Test Community can Rise to the Challenge of Chiplets
Speaker: Jeff Rearick / Senior Fellow, AMD
Location: Laurel Ballroom
Chair: Jing-Jia Liou / National Tsing Hua University

Abstract:
Heterogeneous integration of multiple chiplets into a single package is emerging as the next step in the progression of Moore's Law. Though this technique shows great promise as a platform for many products, it is accompanied by many new challenges, including several for the test community. This presentation will review the motivation for chiplet-based architectures and show a few examples, discuss some specific challenges associated with testing chiplets and chiplet-based systems, and suggest some activities that the test community must complete to address these issues. The critical role of standardization to create a chiplet ecosystem will be emphasized.

Bio:
Jeff Rearick is a Senior Fellow with Advanced Micro Devices, where he has worked for 16 years leading the DFT Strategy team. Prior to joining AMD, Jeff worked at HP/Agilent for 22 years on DFT methodology and implementation for a variety of microprocessor and networking chips. He served as Editor for the IEEE 1687 standard, currently holds that same role again for the refresh activity for 1687 and well as for both the IEEE P1687.1 and P1687.2 Working Groups, and is a member of the P2427 Working Group. He was a founder of all four of those efforts. He was also a member of the IEEE 1149.6 working group and co-authored the first publication of an implementation of that standard. He has published dozens of other technical papers and presentations, holds over 40 patents, and is an active member of the Test Technology Standards Committee as well as the program committees of the International Test Conference and the European Test Symposium. He earned B.S.E.E and M.S.E.E degrees from Purdue University and the University of Illinois, respectively, and was the recipient of the Bob Madge Innovation Award in 2016 and the Hans Karlsson Award from the IEEE Computer Society in 2018.

Keynote 2

Time: 11/22 10:00-10:50am
Topic: Learning by Failing: Test-Thinking for Impactful Machine Learning
Speaker: Trista Chen / Director, Microsoft
Location: Laurel Ballroom
Chair: Harry Chen / Mediatek Inc.

Abstract:
Machine learning has gained tremendous popularity in recent years due to its capabilities in solving complex problems in almost every walk of life, from facial recognition, financial fraud detection to autonomous driving. However, due to its complexity and "black box" nature, deploying a machine learning system to the real-world setting can be challenging. Albert Einstein has once said "anyone who has never made a mistake has never tried anything new". The usefulness of failing, or failing then learning, has been made popular by a software development methodology called Test Driven Development (TDD). TDD converts software requirements to test cases before software is fully developed. It frames how the software intends to work and can reduce the software bugs for up to 90%. Therefore, in this talk, we invite the audience to join the new test-thinking paradigm. With such a new test-thinking, we wish to not only successfully deploy machine learning systems in the real-world but unleash the true potential of machine learning approaches.

Bio:
Trista is a tech executive and an AI scientist. She is currently Director, AI Research Center at Microsoft in Taipei, with research interests in computer vision (CV), human-centered AI, mixed reality, and health AI. In addition to actively publishing 30+ papers and 110+ patents (issued and pending), she won the world championship in USAID Intelligent Forecasting Competition. Previously, Trista held leadership positions at multinational corporations such as Inventec, Intel, and Nvidia and led two startups from incubation to acquisition. As the Chief AI Officer at Inventec, she led the team to obtain the first batch of ISO-13485 medical quality management certificate in Taiwan with a novel AI Software as a Medical Device (SaMD). In addition, she led a successful real-world smart-manufacturing effort in deploying AI supply chain management, quality assurance, and industry 4.0 solutions to day-to-day production lines with annual revenue of 16B USD. At Intel, Trista facilitated the development the world's most widely adopted CV software, OpenCV, which was downloaded 18 million times as of 2021. At Nvidia, she architected Nvidia's first video processor. Trista received her Ph.D. from Carnegie Mellon University and M.S. and B.S. from National Tsing-Hua University.

Keynote 3

Time: 11/22 11:10-12:00am
Topic: A Paradigm Shift; From Device to System Testing
Speaker: Daniel F. J. Yang / Director, TSMC
Location: Laurel Ballroom
Chair: Jin-Fu Li / National Central University
Abstract:
Heterogeneous integration, or by its simpler name of "3DIC" is adopting on advanced silicon manufacturing by innovative packaging with wafer level process technology to gain its power, performance and area benefit. However the 3DIC architecture will continue to drive the Testing complexity. From the testing categories of testing flow, test content, defect learning, test handling and test application all are new challenges that need innovative approaches for testing fundamental functions; to screen defect, to characterize the performance, to detect failure process. There are many focuses, like KGD/KGS/KGP and SLT test strategy to achieve the lower test cost by optimizing the stacking process. What the industry standard for die level test access, also what the test content to support the trade-off between test patterns, test bandwidth and test quality. The defect learning for advanced silicon and packaging to fast bring up through faster PFA, defect isolation and yield improvement. The test contact while the growing bump count and high speed to achieve an optimized Power Integrity and Signal Integrity for interface design. Even the thermal management and mechanical integrity make the Testing become more difficult. 3DIC testing has to enable the heterogeneous integration with appropriate solutions by new collaboration models across industry parties to ensure its success.

Bio:
Daniel Yang is currently as head of testing technology and service division of TSMC. He established many new operation sites and held various technical and managerial positions in the field of testing over 35 years. As foundry testing, Daniel Yang conducted many technical solutions on the integration of probing interface including probe card technology to enable more test coverage on wafer sort stage. Across the different applications of logic and RF to enable silicon and packaging testability through test characterization, data mining solution and optimized process flow to ensure testing coverage while AI and Automotive testing requiring wafer level known good die and heterogeneous testing solutions.

Industry Session 1

Date: Nov.22, 2022
Time: 13:30-14:30pm
Location: Laurel Ballroom Salon I
Chair: Ting-Pu Tai / Synopsys

Time	Title/Speaker
13:30-13:50	**Industrial Test Challenge in 5/4/3nm** *Anti Tseng / Senior Manager, MediaTek*
13:50-14:10	**Test Quality and Cost Co-optimization and Management** *Ying-Yen Chen / Deputy Director, Realtek*
14:10-14:30	**Memory BIST & Repair Solution for Large Chip** *YanLong Niu / DFT Manager, Iluvatar*

Industry Session 2

Date: Nov.22, 2022
Time: 14:40-15:40pm
Location: Laurel Ballroom Salon I
Chair: Charlie Shih / Cadence

Time	Title/Speaker
14:40-15:00	**Evolution of Multi-Chip(let) Packaging Technologies** *Julian Sun / Product Marketing Director, Cadence*
15:00-15:20	**Paradigm Change in Design Methodology** *Julian Sun / Product Marketing Director, Cadence*
15:20-15:40	**Solving Simulation Challenges with System Design and Analysis** *Charlie Shih / Product Engineering Group Director, Cadence*

Industry Session 3

Date: Nov.22, 2022
Time: 16:00-17:00pm
Location: Laurel Ballroom Salon I
Chair: Wu Yang / Siemens EDA

Time	Title/Speaker
16:00-16:30	**The Test Solutions Addressing the Scalings for Technology, Design and System.** *Wu Yang /* Director, Technical Programs, Siemens EDA
16:30-17:00	**Innovative 3D IC DFT Benefiting Ecosystem** *Wu Yang /* Director, Technical Programs, Siemens EDA

Industry Session 4

Date: Nov.23, 2022
Time: 8:30-9:30am
Location: Laurel Ballroom Salon I
Chair: Hung-Pin Charles Wen / NYCU

Time	Title/Speaker
08:30-08:50	**Exploring Vmin Variability via Post-Silicon Profiling** *Harry H. Chen / IC Testing Scientist, MediaTek*
08:50-09:10	**Practical aspects of Logic and Memory Self-test in Industrial Designs** *Ratheesh Thekke Veetil / Senior DFT Manager, Intel Technology India Pvt Ltd*
09:10-09:30	**AI-Driven System Design, Analysis, and Optimization** *Brian Sung / Country Manager, Taiwan, Cadence*

Special Session

Time: 11/23 09:40-10:40am
Location: Laurel Ballroom Salon I
Chair: Masanori Hashimoto / Kyoto University

Time	Title/Speaker
09:40-10:00	**Evaluation of Device Characteristic Changes in X-Ray Inspection** *Takashi Sato / Professor, Kyoto University*
10:00-10:20	**Test Flow for Soft Error-Induced Malfunction in FPGA-Based Autonomous Driving System Using Virtual Environment** *Wang Liao / Program-specific Researcher, University of Tokyo*
10:20-10:40	**Analysing the Reliability of Neural networks in SRAM-Based FPGAs** *Fernanda Kastensmidt / Professor, Universidade Federal do Rio Grande do Sul (UFRGS)*

Regular Session 1

Time: 11/22 13:30-14:30pm
Topic: Reliable Designs
Location: Laurel Ballroom Salon II
Chair: Shyue-Kung Lu / National Taiwan University of Science and Technology

Time	Title/Authors
13:30-13:50	**A Radiation-Hardened Non-Volatile Magnetic Latch with High Reliability and Persistent Storage** *Aibin Yan, Liang Ding, Zhen Zhou, Zhengfeng Huang, Jie Cui, Patrick Girard and Xiaoqing Wen*
13:50-14:10	**Locating Critical-Reliability Gates for Sequential Circuits based on the Time Window Graph Model** *Weidong Zhu, Jianhui Jiang and Zhanhui Shi*
14:10-14:30	**Fault Securing Techniques for Yield and Reliability Enhancement of RRAM** *Zhi-Jia Liu, Masaki Hashizume and Shyue-Kung Lu*

Regular Session 2

Time: 11/22 13:30-14:30pm
Topic: Secure Scan Chain
Location: Chung Kang Room and Wen Hsin Room
Chair: Sying-Jyan Wang / National Chung Hsing University

Time	Title/Authors
13:30-13:50	**An Obfuscation Scheme of Scan Chain to Protect the Cryptographic Chips** *Huixian Huang, Xiaole Cui, Shuming Zhang, Ge Li and Xiaoxin Cui*
13:50-14:10	**An Authentication-Based Secure IJTAG Network** *Shih-Chun Yeh, Kuen-Jong Lee and Dong-Yi Chen*
14:10-14:30	**A New Access Protocol for Elevating the Security of IJTAG Network** *Gaurav Kumar, Anjum Riaz, Yamuna Prasad and Satyadev Ahlawat*

Regular Session 3

Time: 11/22 14:40-15:40pm
Topic: Measurement and Calibration for Test
Location: Laurel Ballroom Salon II
Chair: Jiun-Lang Huang / National Taiwan University

Time	Title/Authors
14:40-15:00	**High Precision Voltage Measurement System Utilizing Low-End ATE Resource and BOST** *Keno Sato, Takayuki Nakatani, Shogo Katayama, Daisuke Iimori, Gaku Ogihara, Takashi Ishida, Toshiyuki Okamoto, Tamotsu Ichikawa, Yujie Zhao, Kentaroh Katoh, Anna Kuwana, Kazumi Hatayama and Haruo Kobayashi*

15:00-15:20	**On-chip Calibration for High-Speed Harmonic Cancellation-Based Sinusoidal Signal Generators** *Ankush Mamgain, Salvador Mir, Jai Narajan Tripathi and Manuel Barragan*
15:20-15:40	**Enhanced Interconnect Test Method for Resistive Open Defects in Final Tests with Relaxation Oscillators** *Masao Ohmatsu, Yuto Ohtera, Yuki Ikiri, Hiroyuki Yotsuyanagi, Shyue-Kung Lu and Masaki Hashizume*

Regular Session 4

Time: 11/22 14:40-15:40pm
Topic: Aging and Reliability
Location: Chung Kang Room and Wen Hsin Room
Chair: Hao-Chiao Hong / National Yang Ming Chiao Tung University

Time	Title/Authors
14:40-15:00	**Aging Impact of Power MOSFETs in Charger with Different Operation Frequency** *Kuan-Hsun Duh, Cheng-Wen Wu, Ming-Der Shieh, Chao-Hsun Chen and Ming-Yan Fan*
15:00-15:20	**On Correction of A Delay Value Using Ring-Oscillators for Aging Detection and Prediction** *Takaaki Kato, Yousuke Miyake and Seiji Kajihara*
15:20-15:40	**Battery Pack Reliability and Endurance Enhancement for Electric Vehicles by Dynamic Reconfiguration** *Yu-You Chou, Cheng-Wen Wu, Ming-Der Shieh and Chao-Hsun Chen*

Regular Session 5

Time: 11/22 16:00-17:00pm
Topic: Diagnostic and On-line Tests
Location: Laurel Ballroom Salon II
Chair: Shi-Yu Huang / National Tsing Hua University

Time	Title/Authors
16:00-16:20	**Deep Learning-assisted Scan Chain Diagnosis with Different Fault Models during Manufacturing Test** *Utsav Jana, Sourav Banerjee, Binod Kumar, Madhu B., Shankar Umapathi and Masahiro Fujita*
16:20-16:40	**Online Periodic Test of Reconfigurable Scan Networks** *Natalia Lylina, Chih-Hao Wang and Hans-Joachim Wunderlich*
16:40-17:00	**Using Formal Methods to Support the Development of STLs for GPUs** *Nikolaos Deligiannis, Tobias Faller, Josie Esteban Rodriguez Condia, Riccardo Cantoro, Bernd Becker and Matteo Sonza Reorda*

Regular Session 6

Time: 11/22 16:00-17:00pm
Topic: System Security and Trust
Location: Chung Kang Room and Wen Hsin Room
Chair: Satyadev Ahlawat / IIT Jammu

Time	Title/Authors
16:00-16:20	**Intrusion Detection and Obfuscation Mechanism for PUF-Based Authentication** *Sying-Jyan Wang, Katherine Shu-Min Li, Chen-Yeh Lin and Song-Kong Chong*
16:20-16:40	**PointerChecker: Tag-Based and Hardware-Assisted Memory Safety against Memory Corruption** *Xiaofan Nie, Liwei Chen and Gang Shi*
16:40-17:00	**Using Hopfield Networks to Correct Instruction Faults** *Troya Çağıl Köylü, Moritz Fieback, Said Hamdioui and Mottaqiallah Taouil*

Regular Session 7

Time: 11/23 08:30-09:30am
Topic: Advanced Test Generation Methods
Location: Laurel Ballroom Salon II
Chair: Tong-Yu Hsieh / National Sun Yat-sen University

Time	Title/Authors
08:30-08:50	**Two-Dimensional Test Generation Objectives** *Irith Pomeranz*
08:50-09:10	**Selecting Path Delay Faults Through the Largest Subcircuits of Uncovered Lines** *Irith Pomeranz*
09:10-09:30	**Using Fault Detection Tests to Produce Diagnostic Tests Targeting Large Sets of Candidate Faults** *Hari Addepalli, Irith Pomeranz, Enamul Amyeen, Suriyaprakash Natarajan, Arani Sinha and Srikanth Venkataraman*

Regular Session 8

Time: 11/23 08:30-09:30am
Topic: Machine Learning and Test AI
Location: Chung Kang Room and Wen Hsin Room
Chair: Tsung-Chu Huang / National Changhua University of Education

Time	Title/Authors
08:30-08:50	**Hybrid Rule-based and Machine Learning System for Assertion Generation from Natural Language Specifications** *Fnu Aditi and Michael S. Hsiao*
08:50-09:10	**AN-HRNS: AN-Coded Hierarchical Residue Number System for Reliable Neural Network Accelerators** *Wan-Ju Huang, Hsiao-Wen Fu and Tsung-Chu Huang*
09:10-09:30	**A Hardware Trojan Trigger Localization Method in RTL based on Control Flow Features** *Hao Huang, Haihua Shen, Shan Li and Huawei Li*

Regular Session 9

Time: 11/23 09:40-10:40am
Topic: Error Analysis and Tolerance
Location: Chung Kang Room and Wen Hsin Room
Chair: Soon-Jyh Chang / National Cheng Kung University

Time	Title/Authors
09:40-10:00	**FPGA-Based Emulation for Accelerating Transient Fault Reduction Analysis** *Zih-Ming Huang, Dun-An Yang, Jing-Jia Liou and Harry H. Chen*
10:00-10:20	**On No-Reference Error Detection of an Image Stitching System Based on Error-Tolerance** *Tong-Yu Hsieh, Pao-Wei Tsui and Jun-Tsung Wu*
10:20-10:40	**Usable Circuits with Imperfect Scan Logic** *Irith Pomeranz*

Ph.D. Thesis Competition

Time: 11/23 11:00-12:00am
Location: Laurel Ballroom Salon I
Chair: Hiroshi Takahashi / Ehime University

Time	Title/Speaker
11:00-11:20	**Towards Robust Deep Neural Network against Design-time Bugs and Run-time Errors** *Yu Li / The Chinese University of Hong Kong*
11:20-11:40	**Neuron-based Secure and Tunable Design: ASICs, FPGAs, and SIMD processors** *Ankit Wagle / Arizona State University*
11:40-12:00	**Study on the High Reliability of Memory-based Programmable Logic Device** *Xihong Zhou / Ehime University*